UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/667,029	09/18/2003	Merwin H. Alferness	ROC920030085US1	9131

30206 7590 07/21/2010

IBM CORPORATION
ROCHESTER IP LAW DEPT. 917
3605 HIGHWAY 52 NORTH
ROCHESTER, MN 55901-7829

EXAMINER	
NGUYEN, TANH Q	
ART UNIT	PAPER NUMBER
2182	

NOTIFICATION DATE	DELIVERY MODE
07/21/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

rociplaw@us.ibm.com

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/667,029
Filing Date: September 18, 2003
Appellant(s): ALFERNESS ET AL.

Christopher P. Mitchell (RN 54,946)
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed June 15 2009 and October 8, 2009 appealing from the Office action mailed October 20, 2008.

(1) Real Party in Interest

The examiner has no comment on the statement, or lack of statement, identifying by name the real party in interest in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The following is a list of claims that are rejected and pending in the application:

1-23

(4) Status of Amendments After Final

The examiner has no comment on the appellant's statement of the status of amendments after final rejection contained in the brief.

(5) Summary of Claimed Subject Matter

The examiner has no comment on the summary of claimed subject matter contained in the brief.

(6) Grounds of Rejection to be Reviewed on Appeal

The examiner has no comment on the appellant's statement of the grounds of

rejection to be reviewed on appeal. Every ground of rejection set forth in the Office action from which the appeal is taken (as modified by any advisory actions) is being maintained by the examiner except for the grounds of rejection (if any) listed under the subheading "WITHDRAWN REJECTIONS." New grounds of rejection (if any) are provided under the subheading "NEW GROUNDS OF REJECTION."

(7) Claims Appendix

The examiner has no comment on the copy of the appealed claims contained in the Appendix to the appellant's brief.

(8) Evidence Relied Upon

6,098,123	Olnowich	8-2000

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-7, 11; 12-18, 22; 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Olnowich (US 6,098,123).

As per claim 1, Olnowich teaches a method of self-adjusting allocation of memory bandwidth in a network processor system [Abstract, lines 1-4; FIG. 5], comprising:

determining an amount of memory bandwidth of a network processor used by a plurality of data types to transmit data through a plurality of active ports [port A and port B are used to transmit data to and from processor 4; port C and port D are used to

transmit data to and from network 2 - hence four different data types through ports A, B, C, D (col. 1, lines 30-36; FIG. 5); in a first example, ports C and D are active with port C using 50 MB/s and port D using 50 MB/s - hence 100 MB/s of memory bandwidth of the network processor being used by two data types to transmit data through two active ports (col. 3, lines 51-66); in a second example, ports A-D are active with port A-B using 25 MB/s, port C using 25 MB/s and port D using 50 MB/s - hence 100 MB/s of memory bandwidth of the network processor being used by four data types to transmit data through four active ports (col. 3, line 62-col. 4, line 2)];

determining an amount of memory bandwidth of the network processor used by each of a plurality of data types [in the first example, data type of port A uses 0 MB/s, data type of port B uses 0 MB/s, data type of port C uses 50 MB/s, and data type of port D uses 50 MB/s (col. 3, lines 51-66); in the second example, data types of ports A-B use 25 MB/s, data type of port C uses 25 MB/s, and data type of port D uses 50 MB/s];

dynamically adjusting an amount of memory bandwidth allocated to at least one of the plurality of data types based on the determinations [in the first example, data types of ports A-B are dynamically adjusted to 25 MB/s and data type of port C is dynamically adjusted to 25 MB/s - when processor requires the use of adapter memory 18 (col. 3, lines 51-66; FIG. 5); in the second example, data types of ports A-B are dynamically adjusted to 75 MB/s when port D becomes inactive; in an alternative of the second example, data types of ports A-B are dynamically adjusted to 50 MB/s and data type of port C is dynamically adjusted to 50 MB/s when port D becomes inactive].

Alternatively, data types of ports A-B are interpreted as a nodal processor data

type - hence the above system comprising three data types and four ports, instead of four data types and four ports.

As per claims 2-7, 11, Olnowich teaches the total amount of memory bandwidth of the network processor used by the plurality of data types being configurable [col. 3, lines 26-col. 4, line 4];

determining whether memory bandwidth may be allocated to at least one of the plurality of data types [col. 3, lines 61-66];

determining a difference between a maximum amount of memory bandwidth of the network processor that may be used by the plurality of data types (i.e. 100 MB/s) and a total amount of memory bandwidth of the network processor currently used by the plurality of data types [in the first example, when it is determined that there is no remaining bandwidth (i.e. when the difference between maximum amount of memory bandwidth and the total amount of memory bandwidth currently used by the plurality of data types is zero), data types of ports A-B are dynamically adjusted to 25 MB/s and data type of port C is dynamically adjusted to 25 MB/s; in the second example, when it is determined that there is no remaining bandwidth, data types of ports A-B are dynamically adjusted to 75 MB/s when port D becomes inactive (or in the alternative, data types of ports A-B are dynamically adjusted to 50 MB/s and data type of port C is dynamically adjusted to 50 MB/s when port D becomes inactive);

determining whether a port for transmitting data of at least one of the plurality data types may be activated [ports A-B may be activated (col. 3, lines 61-66)];

determining a number of active ports of the network processor used to transmit

data of each of the plurality of data types (in the first example, port C and port D are active; in the second example, ports A-B, port C and port D are active); and determining an amount of memory bandwidth allocated to each active port for each of the plurality of data types (in the first example, port C is allocated 50 MB/s and port D is allocated 50 MB/s; in the second example, ports A-B are allocated 25 MB/s [note that if only port A of ports A-B is active, then port A is allocated 25 MB/s; alternatively if only port B of ports A-B is active, then port B is allocated 25 MB/s], port C is allocated 25 MB/s and port D is allocated 50 MB/s);

the amount of memory bandwidth allocated to each active port for a data type is the same (in the first example - port C is active and is allocated 59 MB/s, port D is active and is allocated 50 MB/s).

dynamically activating and deactivating a port for transmitting data of at least one of the plurality of data types (in the first example, ports A-B are dynamically activated; in the second example, port D is dynamically deactivated).

As per claim 12, Olnowich teaches an apparatus [3, FIG. 1] comprising:

a port activation logic [4, 28, 30 - FIG. 5], adapted to couple to a memory [18, FIG. 5] of a network processor [3, FIG. 1] and to interact with the memory so as to:

determine an amount of memory bandwidth of the network processor used by a plurality of data types to transmit data through a plurality of active ports; determine an amount of memory bandwidth of the network processor used by each of the plurality of data types; and dynamically adjust an amount of memory bandwidth allocated to at least one of the plurality of data types based on the

determinations (see the rejection of claim 1 above).

As per claims 13-18, 22, see the rejections of claim 12 and claims 2-7, 11 above.

As per claim 23, Olnowich teaches a network processor system [FIG. 1] comprising:

a memory [18, FIG. 5]; and

a network processor [3, FIG. 1] coupled to the memory, the network processor comprising:

a memory controller [4, 28, 30 - FIG. 5];

a plurality of ports [ports A-D, FIG. 5]; and

a port activation logic, coupled to the memory controller, the plurality of ports and the memory, and adapted to interact with the memory so as to determine an amount of memory bandwidth of the network processor used by a plurality of data types to transmit data through a plurality of active ports; determine an amount of memory bandwidth of the network processor used by each of the plurality of data types; and dynamically adjust an amount of memory bandwidth allocated to at least one of the plurality of data types based on the determinations (see the rejection of claim 12 above).

Claims 8-10, 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olnowich.

Olnowich does not specifically teach the amount of memory bandwidth allocated to each active port for an ATM protocol data type being configurable. Olnowich does

not specifically teach the plurality of data types including at least one of an ATM protocol data type and an Ethernet protocol data type. Olnowich does not specifically teach the Ethernet protocol data type includes at least one of a Gigabit Ethernet data type and a Fast Ethernet data type. Essentially, Olnowich teaches a plurality of nodes communicating over an interconnection network [col. 1, lines 9-14; FIG. 1], but does not specify the type of network.

It would have been obvious to one of ordinary skill in the art at the time the invention was made for Olnowich to use an ATM protocol data type in order to properly communicate in an ATM interconnection network because it was known in the art to use an ATM protocol data type to properly communicate in an ATM interconnection network

It would also have been obvious to one of ordinary skill in the art at the time the invention was made to use an Ethernet protocol data type in order to properly communicate in an Ethernet interconnection network because it was known in the art to use an Ethernet protocol data type to properly communicate in an Ethernet interconnection network; and further to use a Fast Ethernet data type for high-speed applications in the Ethernet interconnection network and/or to use a Gigabit Ethernet data type for applications that requires even higher speed than the Fast Ethernet data type in the Ethernet interconnection network because it was known in the art to use such data types for such applications.

(10) Response to Argument

A PRIMA FACIE CASE OF ANTICIPATION OF CLAIMS 1-7, 11, 12-18, 22 AND 23 HAS NOT BEEN ESTABLISHED.

Appellants argue that Olnowich fails to disclose "determining an amount of memory bandwidth of a network processor used by a plurality of data types".

A. Appellants indicates on pages 7-8 of the Appeal Brief that:

> *At page 4, the present application notes that in the art,*
>
> *memory bandwidth may cause a delay in the transmission of data of certain data types from a first output port while it is retrieving data to be transmitted from a second output port. Because a delay (e.g., an underrun) in the transmission of data of a certain data type (e.g., Fast Ethernet or Gigabit Ethernet, etc.) from the output ports corrupts the data, improved methods and apparatus for allocating memory bandwidth to avoid such delays or underruns are desired.*

The present application then notes that "[m]ethods and apparatus for allocating memory bandwidth to avoid delays or underruns while transmitting data of one or more data types are described [in the application]." Id. With regard to data types, the present application notes by way of inclusion that "[t]he data may be of one or more data types, such as ATM, Fast Ethernet, and/or Gigabit Ethernet." Id.

Appellants appear to rely on the above indications to suggest that Fast Ethernet is one data type and Gigabit Ethernet is another data type; that one or more data types are described in the application; and that the data may be one or more data types, such as ATM, Fast Ethernet, and/or Gigabit Ethernet.

The examiner agrees that **in one interpretation**, Fast Ethernet is one data type and Gigabit Ethernet is another data type.

The examiner also agrees that one or more data types are described in the application. Note however that that "one or more data types" suggests the possibility of more than one data types. Note also that "one or more data types" also suggests the possibility of only one data type. The indication *"[m]ethods and apparatus for allocating memory bandwidth to avoid delays or underruns while transmitting data of one or more*

data types are described [in the application]." would suggest "[m]ethods and apparatus for allocating memory bandwidth to avoid delays or underruns while transmitting data of **one data type** are described [in the application]" – **hence not requiring a plurality of data types**.

The examiner also agrees that the data may be one or more data types, such as ATM, Fast Ethernet, and/**or** Gigabit Ethernet. Note however that *"[t]he data may be of one or more data types, such as ATM, Fast Ethernet, and/or Gigabit Ethernet"* suggests the possibility of "[t]he data may be of **more than one data types**, such as ATM, Fast Ethernet, **or** Gigabit Ethernet" – hence a plurality of data types being ATM, a plurality of data types being Fast Ethernet, **or** a plurality of data types being Gigabit Ethernet (emphasis on "**or**"). **Since there is no explicit definition of data types in the specification**, it is possible for a plurality of data types being ATM, for a plurality of data types being Fast Ethernet, **or** for a plurality of data types being Gigabit Ethernet – **hence a plurality of data types being of the same type.**

In addition, **appellants disclose in the specification "Because both Fast Ethernet and Gigabit Ethernet data are types of Ethernet data" (at page 10, lines 20-21)**. Since Fast Ethernet data is Ethernet data at one speed (100 Mbps – page 9, lines 6-16) and since Gigabit Ethernet data is Ethernet data at another speed (1000 Mbps (10X100 Mbps) – page 9, lines 6-16), **the specification suggests data at one speed being of one data type, and data at another speed being of another data type.**

Still further, claim 9 recites "wherein the plurality of data types includes **at least**

one of an ATM protocol data type and an Ethernet protocol data type". Claim 20 also recites the same limitation. The limitation suggests the possibility of the plurality of data types including only an ATM protocol data type, **or** the possibility of the plurality of data types including only an Ethernet protocol data type **(emphasis on "or" suggested by "at least one of") - hence a plurality of data types being of the same type.**

Furthermore, claim 10 recites "wherein the Ethernet protocol data type includes **at least one of** a Gigabit Ethernet data type and a Fast Ethernet data type". Claim 21 also recites the same limitation. The limitation suggests the possibility of the plurality of data types including only a Gigabit Ethernet data type, **or** the possibility of the plurality of data types including only a Fast Ethernet data type **(emphasis on "or" suggested by "at least one of") - hence a plurality of data types being of the same type.**

Appellants' disclosure, therefore, does not preclude data of the same type being transmitted at different rates from being considered as data of a plurality of data types – hence does not preclude data being transmitted using different ports and at different rates from being considered as data of a plurality of data types. It also appears that appellants' disclosure does not even preclude data being transmitted using different ports from being considered data of a plurality of types (as discussed above, appellants' disclosure suggests a plurality of data types being of the same type).

B. Appellants indicates on page 8 of the Appeal Brief that:

In contrast to these specifically addressed data types, the Office Action points to four (4) ports discussed in the cited passages of Olnowich for disclosing four different types of data. Specifically, the Office Action contends:

port A and port B are used to transmit data to and from processor 4; port C and port D are used to transmit data to and from network 2 - hence four different data types through ports A, B, C, D (col. 1, lines 30-36; FIG. 5)

Additionally, the Advisory Action points to data being slowed from one speed to another speed. However, neither the function of a port (send/receive), the destination of its data (processor/network), nor the slowing of the transmission speed of data have been shown by the Office to equate to "a plurality of data types." That is, these passages have not been shown to disclose anything other than one type of data being transmitted using four (4) different ports.

Appellants respectfully note that the burden is on the Office, not the Appellant, to establish a prima face case. In this instance, the burden is on the Office to establish that ports A-D transmit more than one type of data. Appellants respectfully submit that the Office has not yet met this burden.

Appellants argue that Olnowich fails to disclose "determining an amount of memory bandwidth of a network processor used by a plurality of data types", essentially because the plurality of data types are of the same data type being transmitted using four different ports.

The arguments are not persuasive because appellants' disclosure does not preclude the plurality of data types being data of the same type being transmitted using different ports – as discussed above. Olnowich discloses port A and port B being used to transmit data to and from processor 4; port C and port D being used to transmit data to and from network 2 - hence four different data types through ports A, B, C, D (col. 1, lines 30-36; FIG. 5), therefore the claimed plurality of data types.

The arguments are also not persuasive appellants' disclosure does not preclude the plurality of data types being data of the same type being transmitted at different rates – as discussed above; and because the examiner considers data sent at a first rate being a first type of data, data sent at a second rate being a second type of data,

data sent at a third rate being a third type of data, data sent at a fourth rate being a fourth type of data (col. 3, lines 51-66; col. 3, line 62-col. 4, line 2).

The arguments are also not persuasive appellants' disclosure does not preclude the plurality of data types being data of the same type being transmitted using different ports at different rates – as discussed above; and because the examiner considers data sent at a first rate using a first port being a first type of data, data sent at a second rate using a second port being a second type of data, data sent at a third rate using a third port being a third type of data, data sent at a fourth rate using a fourth port being a fourth type of data (col. 3, lines 51-66; col. 3, line 62-col. 4, line 2).

The arguments are further not persuasive because appellant's arguments are misplaced when appellants suggest that the Advisory Action (mailed January 16, 2009) points to data being slowed from one speed to another speed, and the slowing of the transmission speed of data being shown by the Office to equate to "a plurality of data types". The Advisory Action instead suggests the examiner considering data sent at a first rate being a first type of data, data sent at a second rate being a second type of data, data sent at a third rate being a third type of data, data sent at a fourth rate being a fourth type of data (col. 3, lines 51-66; col. 3, line 62-col. 4, line 2) – hence a plurality of data types (as discussed above).

Essentially, the term "data type" in appellants' disclosure can have many interpretations, and applicant has not claimed the invention with sufficient specificity to suggest only one interpretation and to preclude Olnowich from teaching the invention. There is nothing in the claims that preclude Olnowich

from teaching a plurality of data types because:

data sent through a first port can be considered as data of a first type, data sent through a second port can be considered as data of a second type, data sent through a third port can be considered as data of a third type, and data sent through a fourth port can be considered as data of a fourth type - hence a plurality of data types

alternatively - data sent at a first rate can be considered as data of a first type, data sent at a second rate can be considered as data of a second type, data sent at a third rate can be considered as data of a third type, and data sent at a fourth rate can be considered as data of a fourth type - hence a plurality of data types

still alternatively - data sent at a first rate through a first port can be considered as data of a first type, data sent at a second rate through a second port can be considered as data of a second type, data sent at a third rate through a third port can be considered as data of a third type, and data sent at a fourth rate through a fourth port can be considered as data of a fourth type - hence a plurality of data types

The prima facie case of anticipation of claims 1-7, 11, 12-18, 22 and 23 has therefore been established.

A PRIMA FACIE CASE OF OBVIOUSNESS OF CLAIMS 8-10 AND 19-21 HAS NOT BEEN ESTABLISHED.

Appellants essentially argue that claims 8-10 and 19-21 depend on claims 1, 12

and there is no secondary citation that cures the deficiency of the rejection of claims 1, 12. The argument is not persuasive because a prima facie case of anticipation of claims 1 and 12 has been established above.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/TANH Q. NGUYEN/

Primary Examiner, Art Unit 2182

Conferees:

/Tariq Hafiz/
Supervisory Patent Examiner, Art Unit 2182

/Kevin L Ellis/
Supervisory Patent Examiner, Art Unit 2187